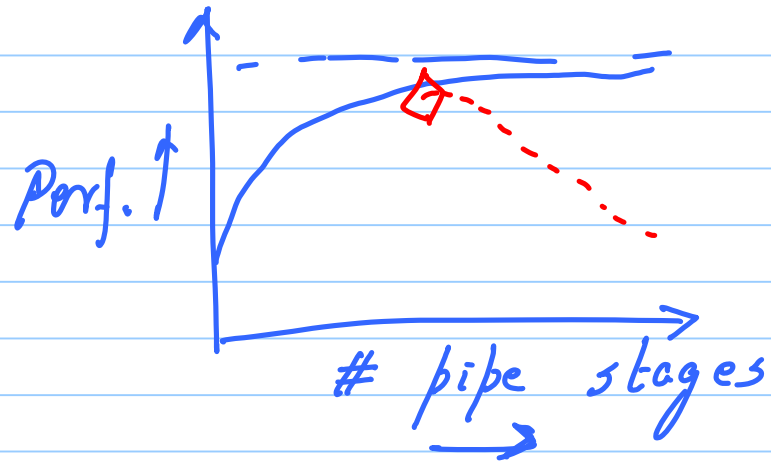


Sept 21st

Note Title

21-09-2011



$$P = IPC \times f \times (\dots)$$

$$T \propto CPI \times t_{clk}$$

Ideal $CPI = 1$

$$CPI = (1 + Kx)$$


constant. \nearrow \nearrow # pipe stages

$$f_{clk} = A + \frac{B}{x}$$

$$f(x) = \left(A + \frac{B}{x}\right) (1 + Kx)$$

$$= A + AKx + \frac{B}{x} + BK$$

$$\frac{\partial f(x)}{\partial x} = AK - \frac{B}{x^2} = 0$$

 $x = \sqrt{\frac{B}{AK}}$

opt # of pipe stages.

A → setup time
+ hold time

B → Algorithmic
Work

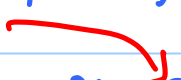
K → stage penalty

Non-Ideal Scenario.

Can we process one Inst. every cycle?

1) Data Hazard.

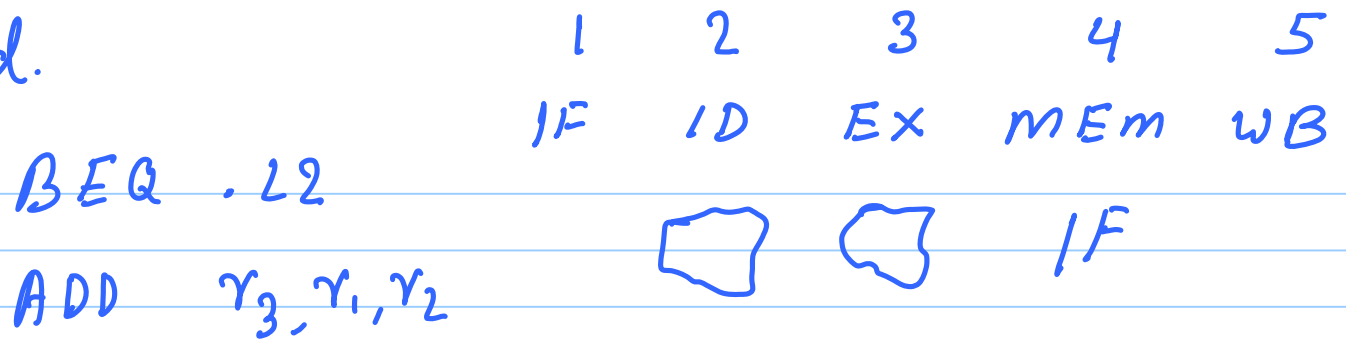
1) ADD r_1, r_2, r_3
2) ADD r_4, r_5, r_1



1) IF ID EX MEM WB
2) IF (ID) EX

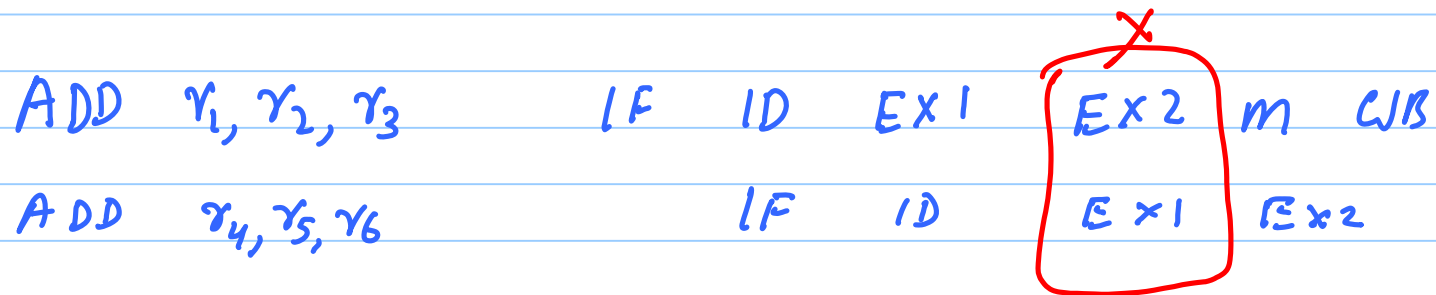
Bubbles in the pipeline

2) Control Hazard.



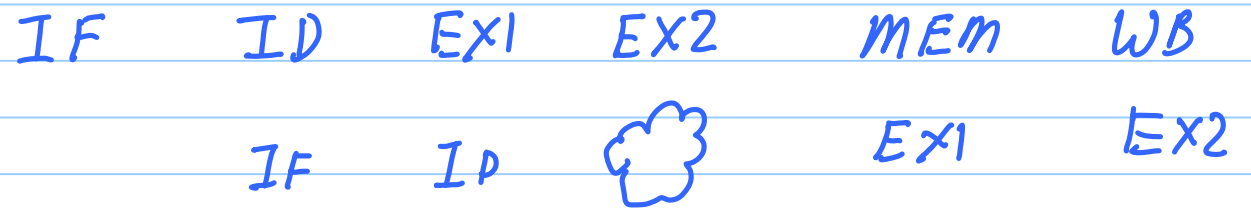
3) Structural Hazard

Assume EX stage is split into two parts EX1 and EX2



What if you have one non-pipelined adder?

Solution:



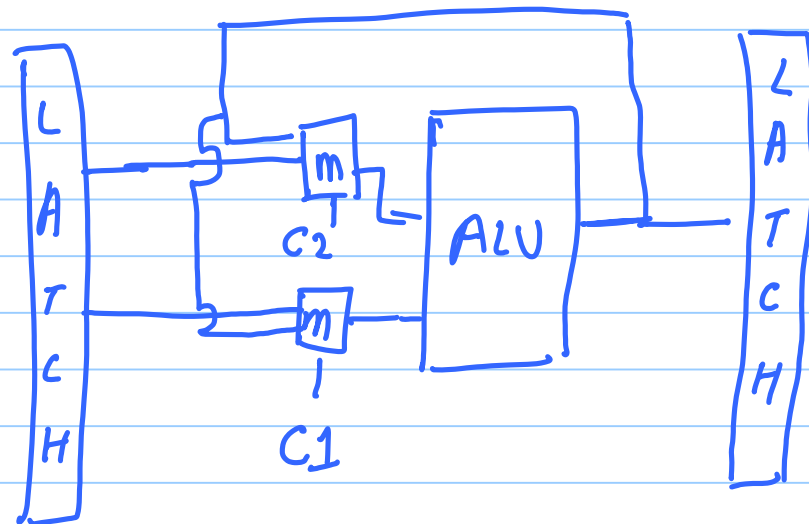
Forwarding.

ADD r_1, r_2, r_3

IF ID EX MEM WB

ADD r_5, r_1, r_4

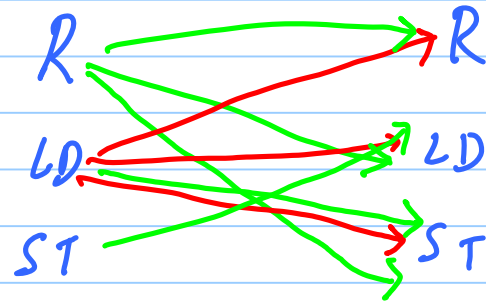
IF ID \rightarrow EX MEM



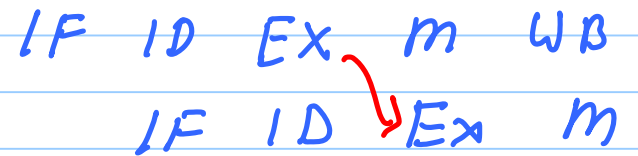
C1 and C2

has to be set appropriately.

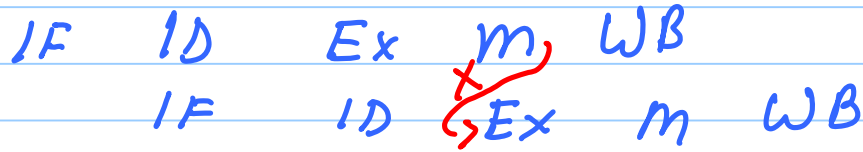
🚩 Forwarding Avoids Data Hazards



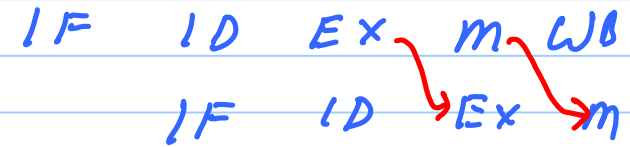
R → LD



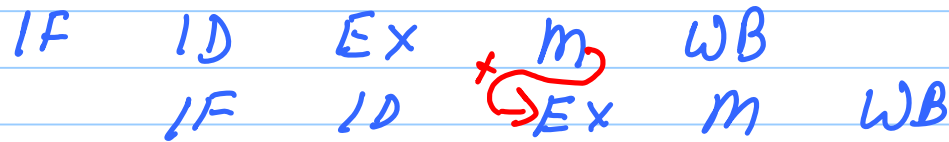
LD → R

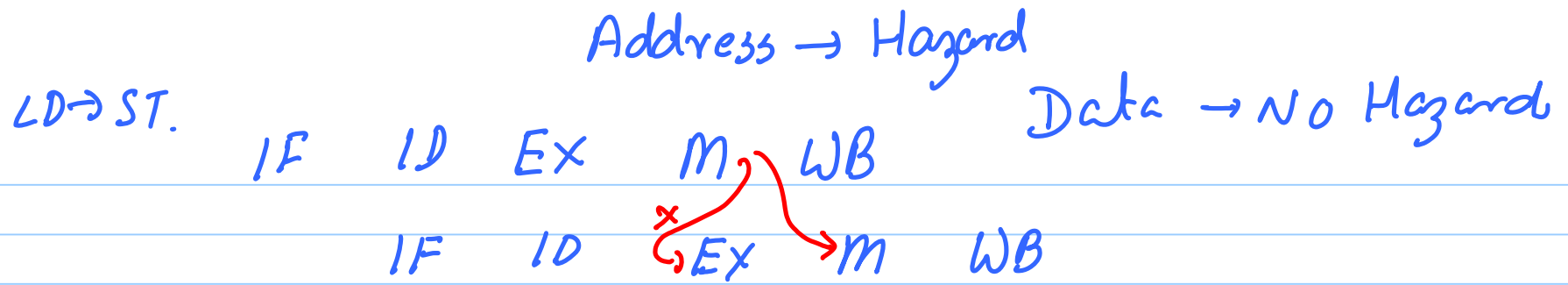


R → ST

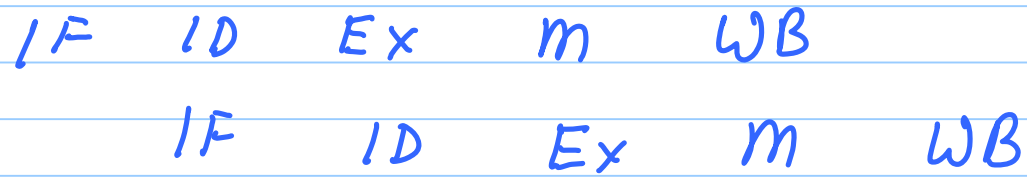


LD → LD





ST → LD



Forwarding Data Path

IF ID EX MEM WB

IF ID (safe)

IF ID (?)

Assumption in MIPS Pipeline.

WB → ID

